REMARKS

Applicants have amended their claims in light of the restriction requirement in the Office Action mailed July 27, 2006, and Response thereto filed August 25, 2006, and in order to further define various aspects of the present invention. Specifically, Applicants have amended claim 19 to be in independent form, incorporating therein subject matter of claim 1, and have provided sub-paragraphing therein. Moreover, Applicants have amended claims 2-12 to be dependent on claim 19, and to recite the "method". Thus, while claims 2-12 have been provided with the status identifier "Withdrawn" in light of the Office Action mailed November 16, 2006, it is respectfully submitted that in light of present amendments to claims 2-12, claims 2-12 fall within the elected group of claims, and must be considered on the merits in the above-identified application. Of course, upon consideration of claims 2-12 on the merits, the status identifiers thereof will be revised to reflect consideration of these claims on the merits.

Moreover, Applicants are adding new claims 21-31 to the application. Claim 21, dependent on claim 20, recites that the step of electrically connecting the semiconductor die onto an exposed surface of the wiring circuit includes bonding the semiconductor die to the die pad and wire bonding the semiconductor die and the inner lead with wires. Claim 22, dependent on claim 19, recites that the step of peeling off the adhesive film is performed at a temperature in a range of 0°C to 250°C; and claims 23-25, each dependent on claim 19, further define the 90 degree peel strength between the resin layer A and the metal sheet prior to the processing of the metal sheet. Claims 26 and 27, dependent respectively on claims 19 and 26, define the 90 degree peel strength at 25°C between the resin layer A and the wiring circuit immediately before carrying out the molding step; and claim 28, dependent on

claim 19, recites the further step of heating prior to the molding step so as to increase adhesive strength between the resin layer A and the wiring circuit. Claims 29-31, each dependent on claim 19, further define the 90 degree peel strengths between the resin layer A and the wiring circuit and between the resin layer A and the molding compound.

In connection with the newly added claims, note, for example, pages 6 and 8-12, of Applicants' specification.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the prior art applied by the Examiner in rejecting claims in the Office Action mailed November 16, 2006, that is, the teachings of the U.S. Patents to Fjelstad, No. 6,856,235, to Fukumoto, et al., No. 6,879,026, and to Lin, et al., No. 5,273,938, under the provisions of 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method for producing a semiconductor device as in the present claims, having the steps (a)-(e) as set forth in claim 19, and using an adhesive film which comprises a support film and a resin layer A formed on one side or both sides of the support film, the 90 degree peel strength between the resin layer A and a metal sheet (processed to give a wiring circuit) laminated to the adhesive film, prior to the processing of the metal sheet, being 20N/m or greater at 25°C, and the 90 degree peel strengths, after molding, between the resin layer A and the wiring circuit and between the resin layer A and the molding compound both being 1000N/m or less at at least one point in the temperature range of 0°C to 250°C. Note claim 19.

As will be shown in the following, it is respectfully submitted that these applied references do not disclose, nor would have suggested, the use of the adhesive film in the process as in the present claims, wherein such adhesive film has the recited 90 degree peel strengths between the resin layer A of the adhesive film and various structures, as in the claims, and advantages thereof.

Furthermore, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such method as in the present claims, having features as discussed previously in connection with claim 19, and, additionally (but not limited to), wherein the wiring circuit includes a plurality of patterns each having a die pad and an inner lead, and wherein the molded wiring circuit laminated with the adhesive film is divided to give a plurality of semiconductor devices each having one semiconductor die (see claim 20); in particular, wherein the step of electrically connecting the semiconductor die onto an exposed surface of the wiring circuit includes bonding the semiconductor die to the die pad and wire bonding the semiconductor die and the inner lead with wires (see claim 21).

Moreover, it is respectfully submitted that these applied references do not disclose, nor would have suggested, such method as in the present claims, having features of claim 19 as discussed previously, and, in addition (but not limited to), wherein the 90 degree peel strengths between the resin layer A and the wiring circuit and between the resin layer A and the molding compound after molding are both 1000N/m or less at at least one point in the temperature range of 100°C-250°C (see claim 2); and/or further definition of the 90 degree peel strengths between the resin layer A and the wiring circuit and between the resin layer A and the molding compound, as in claims 3 and 29-31; and/or glass transition temperature of the resin

layer A and temperature at which the resin layer A shows a 5wt% loss, as in claims 4 and 5, respectively, or elastic modulus of resin layer A as in claim 6; and/or specific materials of the resin layer A as in claims 7 and 8; and/or further definition of the 90 degree peel strength between the resin layer A and the metal sheet prior to the processing of the metal sheet, as in claims 23-25; and/or the 90 degree peel strength at 25°C between the resin layer A and the wiring circuit immediately before carrying out the molding step, as in claims 26 and 27; and/or wherein the step of peeling off the adhesive film is performed at a temperature in a range of 0°C to 250°C (see claim 22); and/or material of the support film of the adhesive film, as in claim 9; and/or ratio of thickness of the resin layer A to thickness of the support film, as in claim 10; and/or the additional step of heating before the molding step, as in claim 28.

Furthermore, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such method as in the present claims, including use of the adhesive film as discussed previously in connection with claim 19, and wherein the resin layer A, which has adhesion, is formed on one side of the support film, and a resin layer B having no adhesion and an elastic modulus at 230°C of 10MPa or greater is formed on the opposite side thereof (see claim 11); and/or wherein the thickness of the adhesive film is 200μm or less (see claim 12).

The invention being considered on the merits in the above-identified application is directed to a method for producing a semiconductor device, including use of an adhesive film that enables a semiconductor package to be produced with high workability.

Recently, a method in which, after an adhesive tape is laminated to one side of a lead frame, a chip is mounted on the opposite side of the lead frame, and is wire bonded and molded, and subsequently the adhesive tape is peeled off, has been proposed. As described in the first full paragraph on page 2 of Applicants' specification, as another method for producing a semiconductor package, a method has been proposed in which, after a metal layer is formed on a temporary support substrate, a circuit is formed, and a chip is mounted, wire bonded, and molded, the temporary support substrate then being peeled off. However, it is not clear from the proposed method the necessary properties for the temporary support substrate.

Against this background, Applicants provide a method utilizing a specified adhesive film as a temporary support substrate, such that a resin molding compound utilized during a molding step is prevented from going around a wiring circuit of the device and the support substrate, and wherein glue residue is prevented from being present on the wiring circuit after peeling off of the support substrate. Applicants have found that by utilizing an adhesive film utilizing a support film and a resin layer A formed on one or both sides of the support film, such resin layer A having specified 90 degree peel strengths at specified points in the manufacturing process with specified components adjacent thereto, the glue residue and undesirable passage of molding compound or other processing materials can be avoided. Specifically, by use of a 90 degree peel strength between the metal sheet and the resin layer A of at least 20N/m, circuit formation defects such as circuit erosion due to penetration of an etching solution during processing of the metal sheet can be avoided; and, moreover, even when the wiring circuit is narrow, peeling off of the adhesive film during a step in which the wiring circuit laminated with the adhesive film is washed or transported, can be avoided. Moreover, entry of molding resin between the wiring

circuit and the resin layer A during the molding step can be avoided. Note the paragraph bridging pages 8 and 9 of Applicants' specification, particularly page 9, lines 11-21.

In addition, by using an adhesion film having a 90 degree peel strength between the resin layer A and the wiring circuit immediately before carrying out the molding step as in various of the present claims, molding resin entering between the wiring circuit and the resin layer A during the molding step can be avoided. See the first full paragraph on page 10 of Applicants' specification.

Furthermore, by having a 90 degree peel strength between the resin layer A and the wiring circuit and between the resin layer A and the molding compound as in the present claims, stress on the wiring circuit for the molding compound, giving rise to the problem of breakage, can be avoided. Note the first full paragraph on page 12 of Applicants' specification.

As to advantages achieved by the present invention, attention is respectfully directed to Examples 1-12 on pages 40-52 of Applicants' specification, as compared with Comparative Examples 1-3 on pages 52-55 thereof. It is respectfully submitted that these examples constitute evidence that must be considered in any determination of obviousness. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984).

As stated in the last full paragraph on page 55 of Applicants' specification, it can be seen from the results of the Examples and Comparative Examples that the use of an adhesive film that has a 90 degree peel strength at 25°C from a metal sheet, prior to processing of the metal sheet to give a wiring circuit, of 20N/m or greater, and 90 degree peel strengths from the wiring circuit and a molding compound at at least one point in the temperature range of 0° C-250°C after resin molding of 1000N/m or less, and that can be peeled from the wiring circuit and the

molding compound, can produce a semiconductor package with high workability and productivity without causing problems in any of the steps, including the metal sheet processing step.

Fjelstad discloses a resistor network having multiple different or common values in a single device manufactured using a single sacrificial layer, and a method of forming such resistor network. Such method is described most generally in column 2, lines 2-25. This patent also provides a description of U.S. Patent No. 6,001,671 in, for example, from column 4, line 38 through column 9, line 45. As one alternative method of manufacture in No. 6,001,671, as described in Fjelstad, a sacrificial layer is comprised of a dielectric polymer sheet 100' having a conductive layer 101', typically a thin layer of copper, on one surface of the sacrificial layer 100' (note Figs. 2A-E). An array of conductive pads 110' are next photo-lithographically defined by etching away undesired sections of the conductive layer 101' so that the pads 110' define a central region 114' therebetween. Within the central region 114', a central conductive region 115' may also be defined by the pad-forming lithographic process; and a back surface 122' of a semiconductor chip 120' is then bonded to the conductive region 115' through the use of the thermally conductive die attached adhesive 135'. Chip contacts on the exposed face surface 121' of the chip 120' are then electrically connected to respective pads 110' by wire bonding wires 130' therebetween; and the elements are next encapsulated using a suitable liquid encapsulate for the application and the encapsulate is cured. Portions of the polymer sheet 100' are then removed, as by chemically etching or laser ablation operations, so that the pads 110' and central conductive region 115' are exposed, and the packages may then be diced into either individual packages or multi chip packages. As another embodiment, this patent discloses a sacrificial layer

comprised of a conductive metallic material, a polymer material or a combination of both a conductive metallic material and a polymer material.

Clearly, Fjelstad would have neither disclosed nor would have suggested the presently claimed subject matter, including use of the adhesive film having the various 90 degree peel strengths, and advantages thereof. Noting especially that Fjelstad discloses chemical etching or laser ablation for removing portions of the polymer sheet, this patent would have taught away from the peel strength of the present claims, and advantages thereof.

Furthermore, Fjelstad would have neither disclosed nor would have suggested the other features of the present invention as discussed in the foregoing, and advantages thereof.

It is respectfully submitted that the additional teachings of the secondary references would not have rectified the deficiencies of Fjelstad, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Thus, Fukumoto, et al. discloses a method of processing a non-circuit formed surface of a semiconductor wafer using an adhesive film for protecting the circuit-formed surface of the semiconductor wafer, such method including the steps of adhering an adhesive film for protecting the surface of the semiconductor wafer through the adhesive layer to the circuit-formed surface thereof; processing the non-circuit-formed surface of the semiconductor wafer until its thickness is reduced to 150μm or less; then peeling the adhesive film for protecting the surface of the semiconductor wafer by heating to a temperature within the range of from 50-90°C. See column 4, lines 7-17. The adhesive film for protecting the surface of the semiconductor wafer includes a substrate film that satisfies the requisite (A) of high

rigidity properties wherein the bending resistance value of the film is within the range of 0.08-1.50N at a temperature of 50°C; and at least one of requisites (B) and (C) respectively of properties wherein the bending resistance value of the film at a temperature of 90°C is one third or less of that at a temperature of 50°C and high elastic modulus properties with expansibility by water absorption. See column 3, lines 18-33. Note also column 4, lines 28-39. See column 11, lines 56 and 57; and column 12, lines 1-9, 16 and 17. Note, further, column 15, lines 33 and 34; and column 16, lines 24-34 and 41-46.

Initially, it is noted that Fukumoto, et al. discloses an adhesive film protecting the circuit-forming surface of the wafer. In contrast, Fjelstad discloses manufacturing processes utilizing a sacrificial layer closest to a back surface (non-circuit-forming surface) of the wafer. The adhesive film of Fukumoto, et al. is only provided for protection, while according to Fjelstad as applied by the Examiner the sacrificial layer includes providing wiring thereon. It is respectfully submitted that one of ordinary skill in the art concerned with in Fjelstad would not have looked to the adhesive film of Fukumoto, et al.

Furthermore, even assuming, arguendo, that one of ordinary skill in the art concerned with in Fjelstad would have looked to the teachings of Fukumoto, et al., and even in light of the teachings of Lin, et al., it is respectfully submitted that the teachings of the applied references do not disclose, nor would have suggested, the 90 degree peel strengths as in the present claims, and advantages thereof. In this regard, the contention by the Examiner in the paragraph bridging pages 3 and 4 of the Office Action mailed November 16, 2006, that it would have been obvious to have provided the 90 degree peel strengths as in the present claims in light of the adhesive layer of Fukumoto, et al., "because the layer of Fukumoto is made from the

same group of materials and have overlapping properties (elastic modulus)" is respectfully traversed. It is respectfully submitted that the elastic modulus and the 90 degree peel strength are different properties. The elastic modulus represents rigidity; and, on the other hand, the 90 degree peel strength represents adhesive strength. Even if the elastic modulus of one film is the same as the elastic modulus of another film, it is respectfully submitted that the 90 degree peel strength of one film is not necessarily the same as the 90 degree peel strength of the other film. Especially in view of the unexpectedly better results achieved according to the present invention, having peel strengths as in the present claims, shown by the Examples and Comparative Examples in Applicants' specification, clearly the teachings of Fukumoto, et al. would have neither disclosed nor would have suggested, even in combination with the teachings of the other applied references, the presently claimed subject matter, including 90 degree peel strengths of the resin layer A.

Moreover, it is respectfully submitted that Fukumoto, et al. expressly focuses on properties of the substrate film. Such substrate film includes, e.g., an adhesive layer thereon, forming the adhesive film. It is respectfully submitted that such disclosure in Fukumoto, et al., in connection with specified properties of the substrate film, would have neither disclosed nor would have suggested the 90 degree peel strengths between resin layer A and various structures of the semiconductor device, and advantages thereof, as in the present claims.

Furthermore, the Examiner's reliance on "overlapping properties (elastic modulus)" as a basis for obviousness, set forth in the paragraph bridging pages 3 and 4 of the Office Action mailed November 16, 2006, is again noted. However, it is respectfully submitted that Fukumoto, et al. does not disclose overlapping properties

(elastic modulus). It is respectfully submitted that the elastic modulus in Fukumoto, et al. is an elastic modulus of from 50-90°C, and cannot be directly compared with an elastic modulus at 230°C, as the value of the elastic modulus clearly depends on temperature, as can be seen in the sole figure of Fukumoto, et al.

As can be seen in all of the foregoing, clearly the teachings of Fukumoto, et al., even in combination with the teachings of Fjelstad, and further in combination with the teachings of Lin, et al. (discussed infra), would have neither taught nor would have suggested the presently claimed invention, including, inter alia, 90 degree peel strengths between the resin film A and various structures, and advantages thereof; or other features of the present invention as discussed previously, and advantages thereof.

Lin, et al. discloses resin encapsulating semiconductor devices which have multiple electronic components, and methods for fabricating such devices, wherein a transfer film is provided on which a pattern of conductive traces is formed. A first electronic component is interconnected to the pattern of conductive traces and a first package body is formed to encapsulate the first electronic component and a first portion of the pattern of conductive traces. The transfer pattern is then removed to expose a second portion of the pattern of traces on a bottom surface of the first package body; and a second electronic component is provided on the bottom surface of the first package body. A second package body is formed to encapsulate the second electronic component while leaving the second portion of the pattern of traces exposed. See column 2, lines 14-29. Note also the paragraph bridging columns 2 and 3; column 3, lines 25-27, 35-39 and 57-62; and column 4, lines 9-13, 23-26, 34-37, 44-46 and 57-68.

Even assuming, arguendo, that the teachings of Lin, et al. were properly combinable with the teachings of Fjelstad and Fukumoto, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including use of the adhesive film having the support film and a resin layer A as in the present claims, with the 90 degree peel strengths between the resin layer A and specified components of the semiconductor device, as in the present claims, and advantages thereof; and/or other features of the present invention as discussed previously, and advantages thereof.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Authorization is herein given to charge any shortage in the fees, including extension of time fees and excess claim fees, to Deposit Account No. 01-2135 (Case No. 1204.44601X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

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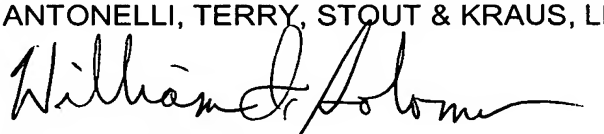

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